AF
2812

DA01036/1363D

PATENT IFW



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Hao Fang et al.

Serial No.: 09/941,370

Filed: August 28, 2001

Group Art Unit: 2812

Before the Examiner: Richard A. Booth

Title: FLASH MEMORY DEVICE AND A METHOD OF FABRICATION THEREOF

## REPLY BRIEF TRANSMITTAL LETTER

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith are three (3) copies of the Reply Brief and an Acknowledgment Postcard.

---

**CERTIFICATION UNDER 37 C.F.R. § 1.8**

I hereby certify that this correspondence (along with any item referred to as being enclosed herewith) is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 21, 2004.

Serena Beller
Signature

Serena Beller
*(Printed name of person certifying)*

No fee is due, however, the Assistant Commissioner is hereby authorized to charge any insufficiency in fees associated with this communication, or credit any overpayment, to Deposit Account No. 01-0365 (DA01036/1363D). **A duplicate copy of this transmittal letter is attached.**

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Attorney for Applicants

By: _____

Robert A. Voigt, Jr.
Reg. No. 47,159

P.O. Box 50784
Dallas, Texas 75201
(512) 370-2832

AUSTIN_1\250906\1
184-P063D1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Hao Fang et al.

Serial No.: 09/941,370

Filed: August 28, 2001

Group Art Unit: 2812

Before the Examiner: Richard A. Booth

Title: FLASH MEMORY DEVICE AND A METHOD OF FABRICATION THEREOF

May 21, 2004

**REPLY BRIEF**

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Reply Brief is being submitted in response to the Examiner's Answer dated May 13, 2004 (Paper No. 19), with a two-month statutory period for response set to expire on July 13, 2004.

**CERTIFICATION UNDER 37 C.F.R. § 1.8**

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 21, 2004.

Serena Beller
Signature

Serena Beller
*(Printed name of person certifying)*

## I. RESPONSE TO EXAMINER'S ARGUMENTS

### A. Response to Examiner's argument, as discussed on page 5 of Paper No. 19, that the Examiner has provided a *prima facie* case of obviousness for combining Cappelletti with Holler.

The Examiner's motivation for modifying Cappelletti with Holler to strengthen the interface between the oxide and silicon substrate by providing a nitrification process in both the core area and the periphery area of the memory device thereby improving the reliability of the dual gate oxide in the core area, as recited in claim 1 and similarly in claim 10, is "because nitridation processes enhance the quality of gate oxides (see col. 5, lines 12-15 of Holler et al.). Paper No. 19, page 5. This motivation is insufficient to support a *prima facie* case of obviousness as discussed below.

The Examiner's motivation appears to have been gleaned from the secondary reference, Holler. In fact, the Examiner cites column 5, lines 12-15 of Holler as support for his motivation. Paper No. 19, page 5. This is not evidence as to why one of ordinary skill in the art with the primary reference, Cappelletti, in front of him would have been motivated to modify Cappelletti with the teachings of the secondary reference, Holler. The Examiner's motivation is motivation for the secondary reference, Holler, to solve its problem. This is not a suggestion to combine the primary reference, Cappelletti, with the secondary reference, Holler. The Examiner must provide evidence as to why one of ordinary skill in the art with Cappelletti in front of him, which teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process (Abstract of Cappelletti), would be motivated to modify Cappelletti with the teachings of Holler, which teaches fabricating contactless memory cells (Abstract of Holler). *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-1434 (Fed. Cir. 2002); *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000). Merely stating what the secondary reference teaches is not evidence for combining a primary reference, Cappelletti, with the secondary reference, Holler. *See Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 1-2 and 10. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Cappelletti, which teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process, with Holler, which teaches fabricating contactless memory cells. *Id.* There is no suggestion in Cappelletti of fabricating contactless memory cells. Since the Examiner has not submitted objective evidence for modifying Cappelletti with Holler, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-2 and 10. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Cappelletti to strengthen the interface between the oxide and silicon substrate by providing a nitrification process in both the core area and the periphery area of the memory device thereby improving the reliability of the dual gate oxide in the core area (Examiner admits that Cappelletti does not teach this limitation). *Id.* There is no suggestion in Cappelletti of strengthening the interface between the oxide and silicon substrate. Neither is there any suggestion in Cappelletti of strengthening the interface between the oxide and silicon substrate by providing a nitrification process in both the core area and the periphery area of the memory device. Since the Examiner has not submitted objective evidence in support of modifying Cappelletti to strengthen the interface between the oxide and silicon substrate by providing a nitrification process in both the core area and the periphery area of the memory device thereby improving the reliability of the dual gate oxide in the core area, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-2 and 10. *Id.*

B. Response to Examiner's argument, as discussed on pages 5-6 of Paper No. 19, that the Examiner has provided a *prima facie* case of obviousness for combining Cappelletti with Wristers.

The Examiner's motivation for modifying Cappelletti with Wristers to strengthen the interface between the oxide and silicon substrate by providing a nitrification process in both the core area and the periphery area of the memory device thereby improving the reliability of the dual gate oxide in the core area, as recited in claim 1 and similarly in

claim 10, is "because nitridation improves the properties of oxides (see col. 3, lines 40-65 of Wristers et al.). Paper No. 19, page 6. This motivation is insufficient to support a *prima facie* case of obviousness as discussed below.

The Examiner's motivation appears to have been gleaned from the secondary reference, Wristers. In fact, the Examiner cites column 3, lines 40-65 of Wristers as support for his motivation. Paper No. 19, page 6. This is not evidence as to why one of ordinary skill in the art with the primary reference, Cappelletti, in front of him would have been motivated to modify Cappelletti with the teachings of the secondary reference, Wristers. The Examiner's motivation is motivation for the secondary reference, Wristers, to solve its problem. This is not a suggestion to combine the primary reference, Cappelletti, with the secondary reference, Wristers. The Examiner must provide evidence as to why one of ordinary skill in the art with Cappelletti in front of him, which teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process (Abstract of Cappelletti), would be motivated to modify Cappelletti with the teachings of Wristers, which teaches a silicon oxynitride (oxynitride) dielectric layer using a process in which nitrogen is incorporated into the dielectric as it is grown upon a silicon substrate (Abstract of Wristers). *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-1434 (Fed. Cir. 2002); *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000). Merely stating what the secondary reference teaches is <u>not</u> evidence for combining a primary reference, Cappelletti, with the secondary reference, Wristers. *See Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 1-2 and 10. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Cappelletti, which teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process, with Wristers, which teaches a silicon oxynitride dielectric layer using a process in which nitrogen is incorporated into the dielectric as it is grown upon a silicon substrate. *Id.* There is no suggestion in Cappelletti of having a silicon oxynitride dielectric layer.

Neither is there any suggestion in Cappelletti of having a silicon oxynitride dielectric layer using a process in which nitrogen is incorporated into the dielectric as it is grown upon a silicon substrate. Since the Examiner has not submitted objective evidence for modifying Cappelletti with Wristers, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-2 and 10. *Id.*

C. Response to Examiner's argument, as discussed on page 6 of Paper No. 19, that the Examiner has provided a *prima facie* case of obviousness for combining Cappelletti with Takebuchi.

The Examiner's motivation for modifying Cappelletti with Takebuchi to strengthen the interface between the oxide and silicon substrate by providing a nitrification process in both the core area and the periphery area of the memory device thereby improving the reliability of the dual gate oxide in the core area, as recited in claim 1 and similarly in claim 10, is "because films of longer endurance are produced." Paper No. 19, page 5. This motivation is insufficient to support a *prima facie* case of obviousness as discussed below.

The Examiner's motivation appears to have been gleaned from the secondary reference, Takebuchi. In fact, the Examiner cites column 1, line 35 – column 2, line 18 of Takebuchi as support for his motivation. Paper No. 19, page 6. This is not evidence as to why one of ordinary skill in the art with the primary reference, Cappelletti, in front of him would have been motivated to modify Cappelletti with the teachings of the secondary reference, Takebuchi. The Examiner's motivation is motivation for the secondary reference, Takebuchi, to solve its problem. This is not a suggestion to combine the primary reference, Cappelletti, with the secondary reference, Takebuchi. The Examiner must provide evidence as to why one of ordinary skill in the art with Cappelletti in front of him, which teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process (Abstract of Cappelletti), would be motivated to modify Cappelletti with the teachings of Takebuchi, which teaches a non-volatile memory element and a p-channel IGFET mounted on a single substrate where the nitride atom density of tunnel insulating film of the non-volatile memory element is

set to be higher than the nitride atom density of a gate insulating film of the p-channel IGFET (Abstract of Takebuchi). *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-1434 (Fed. Cir. 2002); *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000). Merely stating what the secondary reference teaches is not evidence for combining a primary reference, Cappelletti, with the secondary reference, Takebuchi. *See Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 1-2 and 10. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Cappelletti, which teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process, with Takebuchi, which teaches a non-volatile memory element and a p-channel IGFET mounted on a single substrate where the nitride atom density of tunnel insulating film of the non-volatile memory element is set to be higher than the nitride atom density of a gate insulating film of the p-channel IGFET. *Id.* There is no suggestion in Cappelletti of having a non-volatile memory element and a p-channel IGFET mounted on a single substrate. Neither is there any suggestion in Cappelletti of having a non-volatile memory element and a p-channel IGFET mounted on a single substrate where the nitride atom density of tunnel insulating film of the non-volatile memory element is set to be higher than the nitride atom density of a gate insulating film of the p-channel IGFET. Since the Examiner has not submitted objective evidence for modifying Cappelletti with Takebuchi, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-2 and 10. *Id.*

The Examiner further states that the motivation to combine Cappelletti with Takebuchi may come from knowledge generally available to one of ordinary skill in the art. Paper No. 19, page 6. While motivation may come from knowledge generally available to one of ordinary skill in the art, the Examiner must still provide objective evidence that such knowledge was generally available to one of ordinary skill in the art. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). By the Examiner not providing

any objective evidence to support his assertion, the Examiner is merely relying upon his own subjective opinion or at most "common knowledge" and "common sense" which cannot substitute evidence. *In re Lee*, at 1435. Hence, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-2 and 10. *In re Lee*, at 1434.

Further, if the Examiner is relying upon knowledge available to one of ordinary skill in the art in support of his obviousness rejection, the Examiner must ascertain the level of ordinary skill using such factors as outlined in *Environmental Designs, Ltd. v. Union Oil Co.*, 218 U.S.P.Q. 865, 868 (Fed. Cir. 1983). M.P.E.P. §2141.03. Since the Examiner has not ascertained the level of ordinary skill in the art, the Examiner has not presented objective evidence for modifying Cappelletti with Takebuchi and hence has not presented a *prima facie* case of obviousness for rejecting claims 1-2 and 10. *See Environmental Designs, Ltd. v. Union Oil Co.*, 218 U.S.P.Q. 865, 868 (Fed. Cir. 1983); *In re Lee* 61, U.S.P.Q.2d 1430, 1433-1434 (Fed. Cir. 2002).

Further, the Examiner states that "a film of longer endurance would be clearly apparent to one of ordinary skill in the art because this would allow for a device which performs at a high level longer than other devices." Paper No. 19, page 6. The Examiner must submit objective evidence in support of modifying Cappelletti to allow for a gate film of longer endurance which may allow the device to perform at a high level longer (Examiner's motivation). *In re Lee* 61, U.S.P.Q.2d 1430, 1433-1434 (Fed. Cir. 2002). There is no suggestion in Cappelletti of having a gate film of longer endurance. Neither is there any suggestion in Cappelletti of having a gate film of longer endurance which may allow the device to perform at a high level longer. Since the Examiner has not submitted objective evidence for modifying Cappelletti to have a gate film of longer endurance (Examiner's motivation), the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-2 and 10. *Id.*

D. Response to Examiner's argument, as discussed on page 7 of Paper No. 19, that Appellants are arguing that prior art devices are not physically combinable.

Appellants respectfully traverse the Examiner's assertion that Appellants' arguments that the principle of operation of Cappelletti would change when combined with Takebuchi or Holler or Wristers are in essence arguments that the prior art devices are not physically combinable. There are no such arguments made by Appellants. Appellants instead argue that the claimed combination changes the principle of operation of Cappelletti and renders Cappelletti inoperable for its intended purpose. This argument is permissible under M.P.E.P. §2143.01. Further, according to M.P.E.P. §2145, the Examiner cannot cite *In re Keller* to support the assertion that Appellants cannot argue that the claimed combination changes the principle of operation of Cappelletti and renders Cappelletti inoperable for its intended purpose.

Further, the Examiner appears to also be asserting that the Examiner does not have to consider the references in their entirety when combining two or more references in an obviousness rejection. Appellants respectfully traverse the assertion that the entire reference of Takebuchi or Holler or Wristers need not be considered when the Examiner combines them with Cappelletti in an obviousness rejection. The entire reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 U.S.P.Q. 303 (Fed. Cir. 1983); M.P.E.P. §2141.02

E. Response to Examiner's argument, as discussed on pages 6 and 7 of Paper No. 19, that Appellants are attacking references individually where the rejections are based on combinations of references.

Appellants respectfully traverse the assertion that Appellants are attacking the references individually where the rejections are based on combination of references. The Examiner has not listed one example in which Appellants allegedly attack the references individually. Instead, Appellants argue that the references taken singly or in combination do not teach or suggest particular claim limitations. Further, the Examiner cannot ignore

claim limitations, e.g., strengthening the interface by providing a nitrification process in both the core area and periphery area of the memory device subsequent to steps (a) and (b), by simply asserting that Appellants are arguing against the references individually. All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970).

F. Response to Examiner's argument, as discussed on page 7 of Paper No. 19, that a reference that shows a suitability for an intended purpose is a proper motivation to combine references.

Appellants do not contest the assertion that the selection of a known material based on its suitability for its intended use may support a *prima facie* case of obviousness. M.P.E.P. §2144.07. Appellants though are confused as to why this statement is made in connection with the rejection to claims 2 and 10. The Examiner's motivation for modifying Cappelletti with either Takebuchi, Holler or Wristers and in further view of Lee (1) to deposit a layer of type-1 polysilicon in both a core area and a periphery area of a memory device; (2) to deposit a layer of oxide nitride oxide over the layer of type-1 polysilicon; and (3) to remove the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device, as recited in claims 2 and 10, is "because this is shown to be conventional fabrication for memory and peripheral circuits."

The Examiner has not provided any objective evidence that the steps outlined above are conventional fabrication steps. The Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness in rejecting claims 2 and 10. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Cappelletti (1) to deposit a layer of type-1 polysilicon in both a core area and a periphery area of a memory device; (2) to deposit a layer of oxide nitride oxide over the layer of type-1 polysilicon; and (3) to remove the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the

periphery area of the memory device (Examiner admits that Cappelletti does not teach these limitations). *Id.* There is no suggestion in Cappelletti of depositing a layer of type-1 polysilicon in both a core area and a periphery area of a memory device. Neither is there a suggestion in Cappelletti of depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon. Neither is there a suggestion in Cappelletti of removing the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device. Since the Examiner has not submitted objective evidence for modifying Cappelletti to perform the above steps, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2 and 10. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Cappelletti, which teaches producing a flash-EEPROM memory array and associated transistors using the DPCC process, with Lee, which teaches simplifying the CMOS process by reducing the number of photomasks required as well as optimizing the n-channel implants of the array and periphery relative to one another (Abstract of Lee). *Id.* There is no suggestion in Cappelletti of reducing the number of photomasks. Neither is there any suggestion in Cappelletti of optimizing the n-channel implants of the array and periphery relative to one another. Since the Examiner has not submitted objective evidence for modifying Cappelletti with Lee, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2 and 10. *Id.*

G. Other matters raised by the Examiner.

All other matters raised by the Examiner have been adequately addressed above and in Appellants' Appeal Brief and in Appellants' Supplemental Appeal Brief and therefore will not be addressed herein for the sake of brevity.

II. CONCLUSION

For the reasons stated in Appellants' Appeal Brief and in Appellants' Supplemental Appeal Brief and noted above, Appellants respectfully assert that the rejections of claims 1, 2 and 10 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-4 and 10.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Attorneys for Appellants

By: _____
Robert A. Voigt, Jr.
Reg. No. 47,159
Kelly K. Kordzik
Reg. No. 36,571

P.O. Box 50784
Dallas, Texas 75201
(512) 370-2832

AUSTIN_1\250783\1
184-P063D1